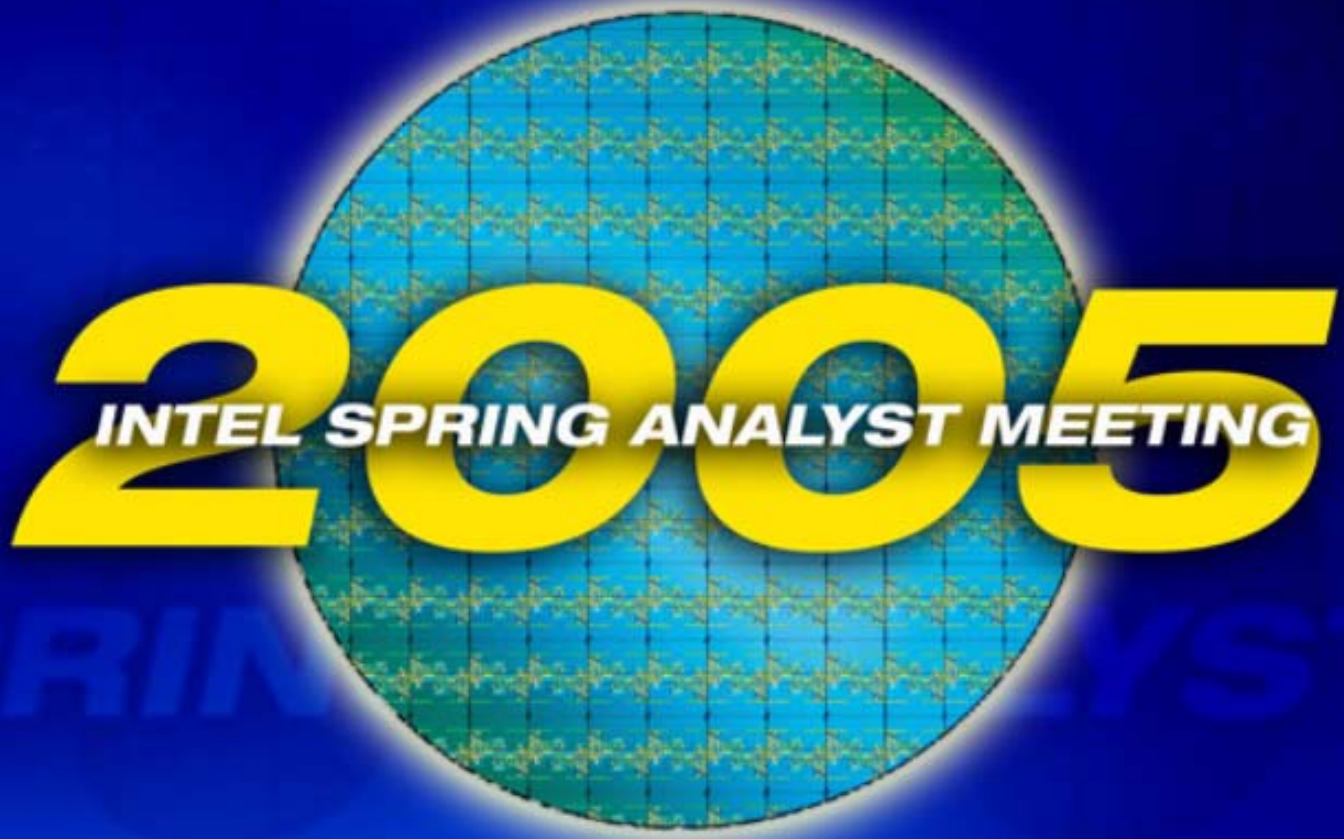


Andy Bryant
Executive Vice President
Chief Financial and Enterprise Services Officer

" I wanted to get across the idea that integrated circuits were a way to make electronics cheap.

You could see the technology was going to let you make more complex things and the costs were going to go down.

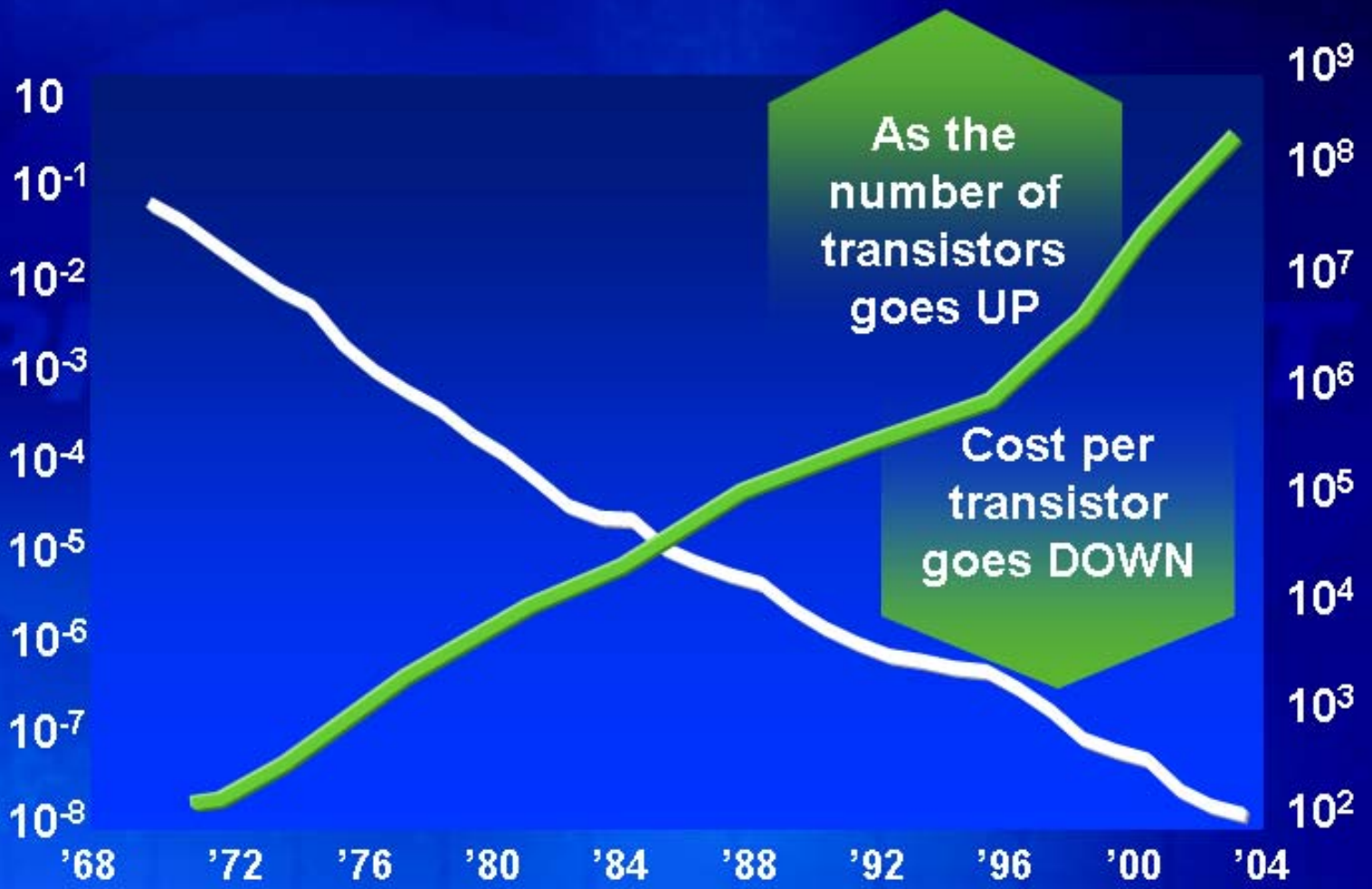
That was really the message I wanted to get across."

Gordon Moore
San Jose Mercury News
April 2, 2005

intel

The Economics of Moore's Law

SCALING + WAFER SIZE + HIGH VOLUME = LOWER COSTS



Source: WSTS/Dataquest/Intel, 3/04

The Fundamental Cost Driver



350nm 200mm | 250nm 200mm | 180nm 200mm | 130nm 200mm | 90nm 300mm | 65nm 300mm *Dual Core*

Twice the circuitry in the same space (architecture innovation)

OR

The same circuitry in half the space (cost reduction)

=

Half the die size than in the prior process

intel

Source: Intel

Scaling Reduces Costs

NO SCALING SCENARIO

- Process R&D stops
- Die size constant
- Wafer costs flat

SCALING SCENARIO

- Increasing process R&D
- ~2 year cycle
- 0.5X area reduction
- Increasing wafer costs
- Lower die costs

COST BENEFIT SENSITIVE TO

- Prolonged unit declines
- Major increases in R&D
- Large wafer cost increases
- Low area reduction



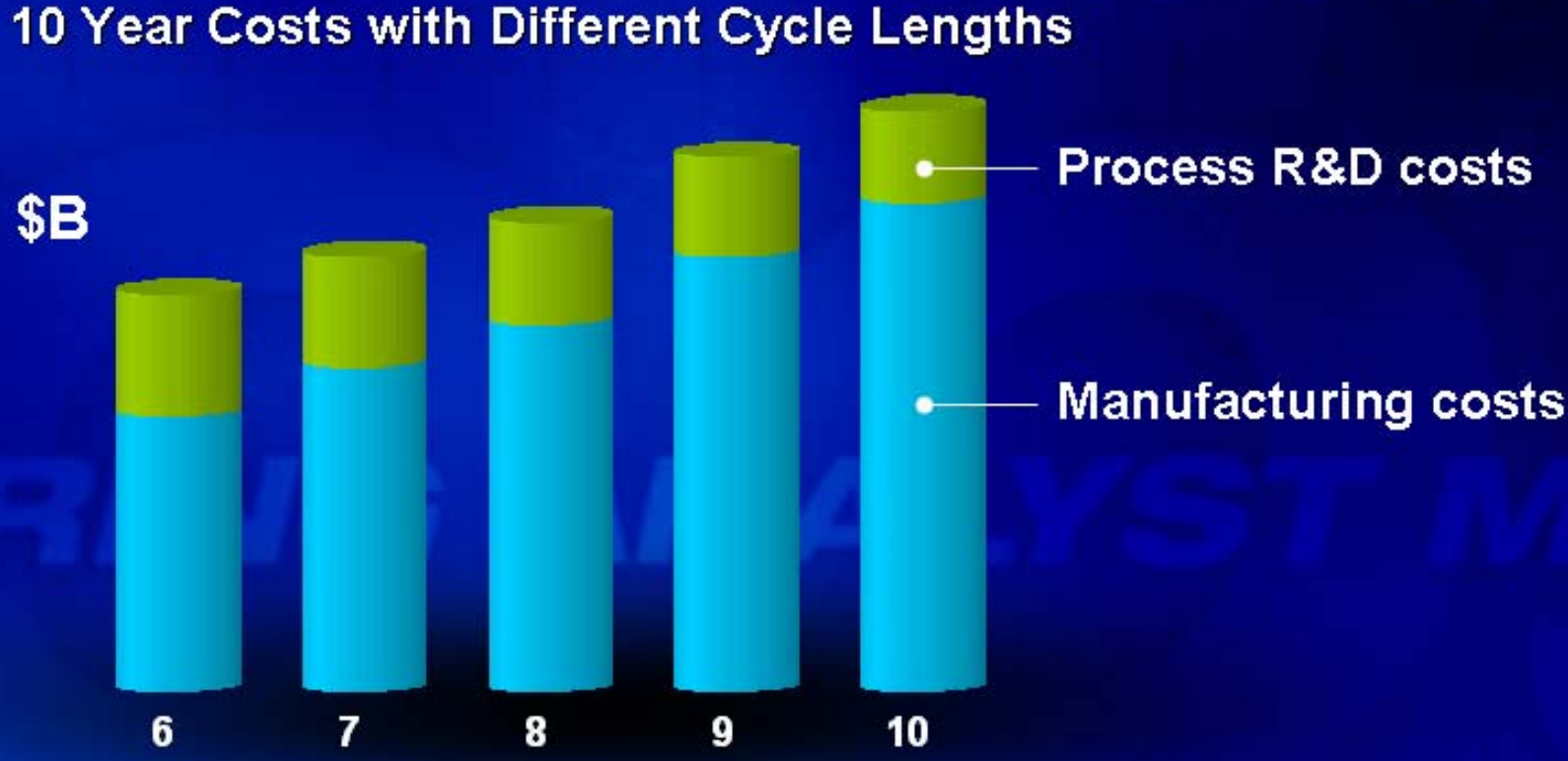
>$8B cost without scaling

Cost benefit captured
in a range of business conditions

intel

Source: Intel

Faster Is Better



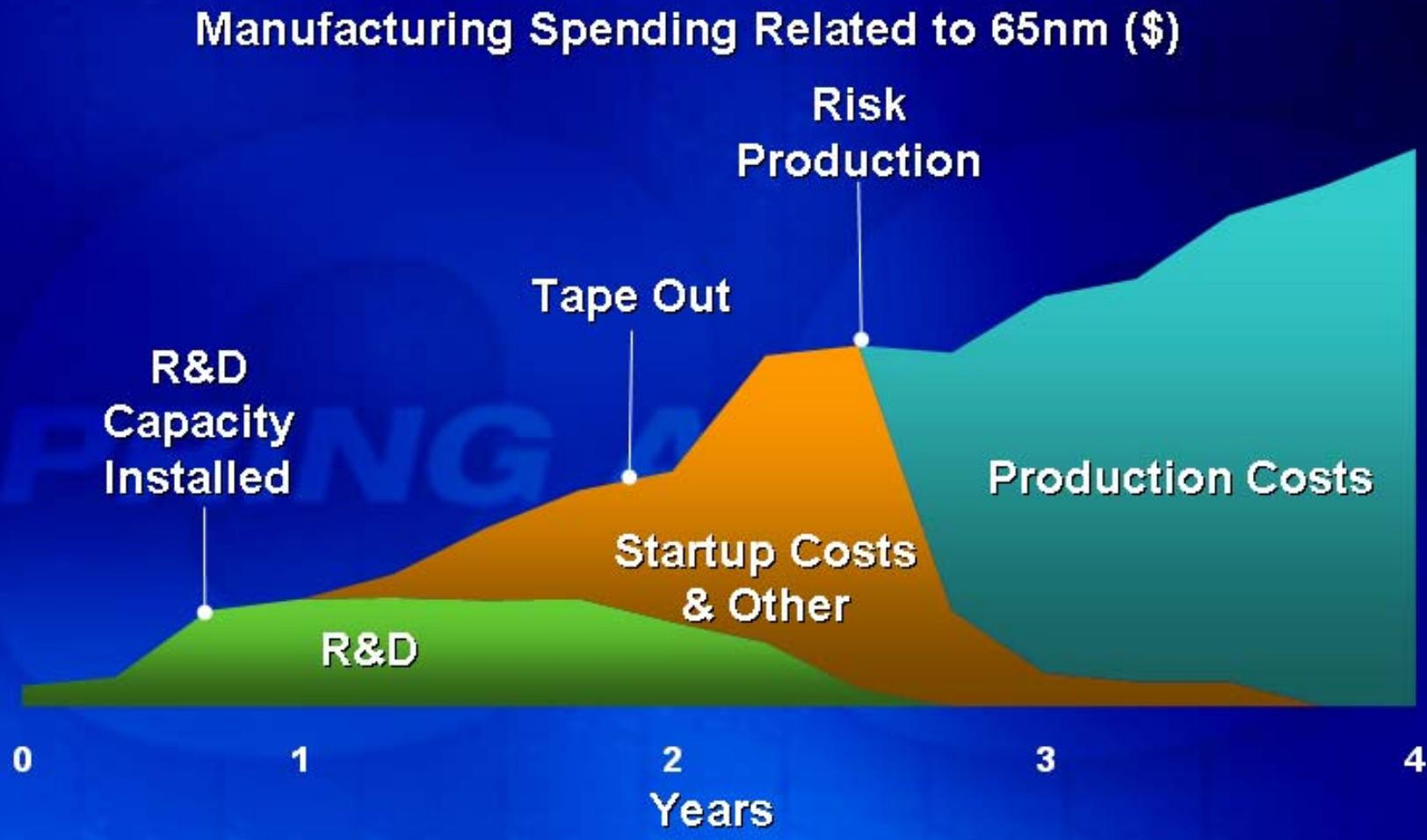
As cycles are extended,
manufacturing costs increase faster than R&D costs

Benefit extends to chipsets and memory

Practical limitations with suppliers and staffing

Source: Intel

65nm Spending Progression



A structured cycle to deliver high volume, high yield output

intel

Source: Intel

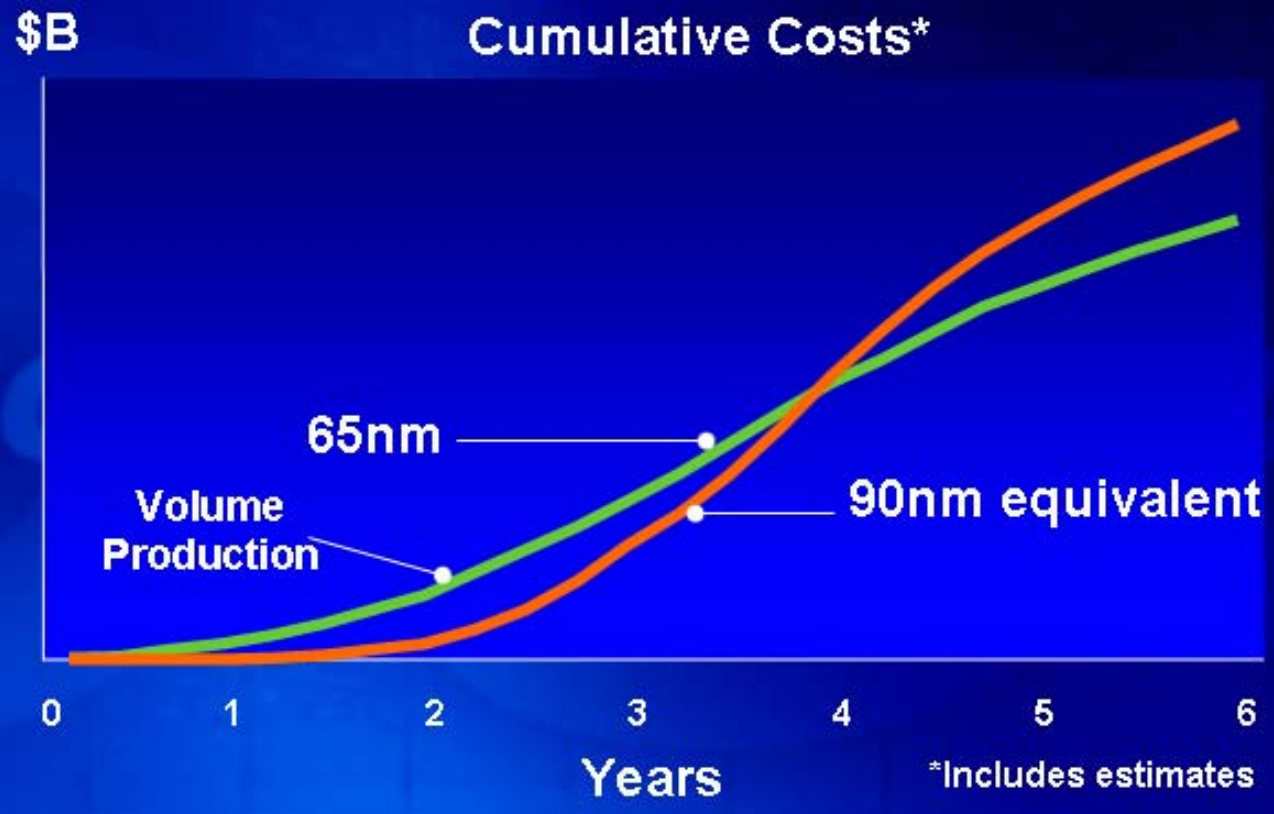
The Case of 65nm

65nm

- R&D
- Startup costs
- Production costs

90nm equivalent roadmap

- R&D
- Startup costs
- Production costs
- 2 additional fabs

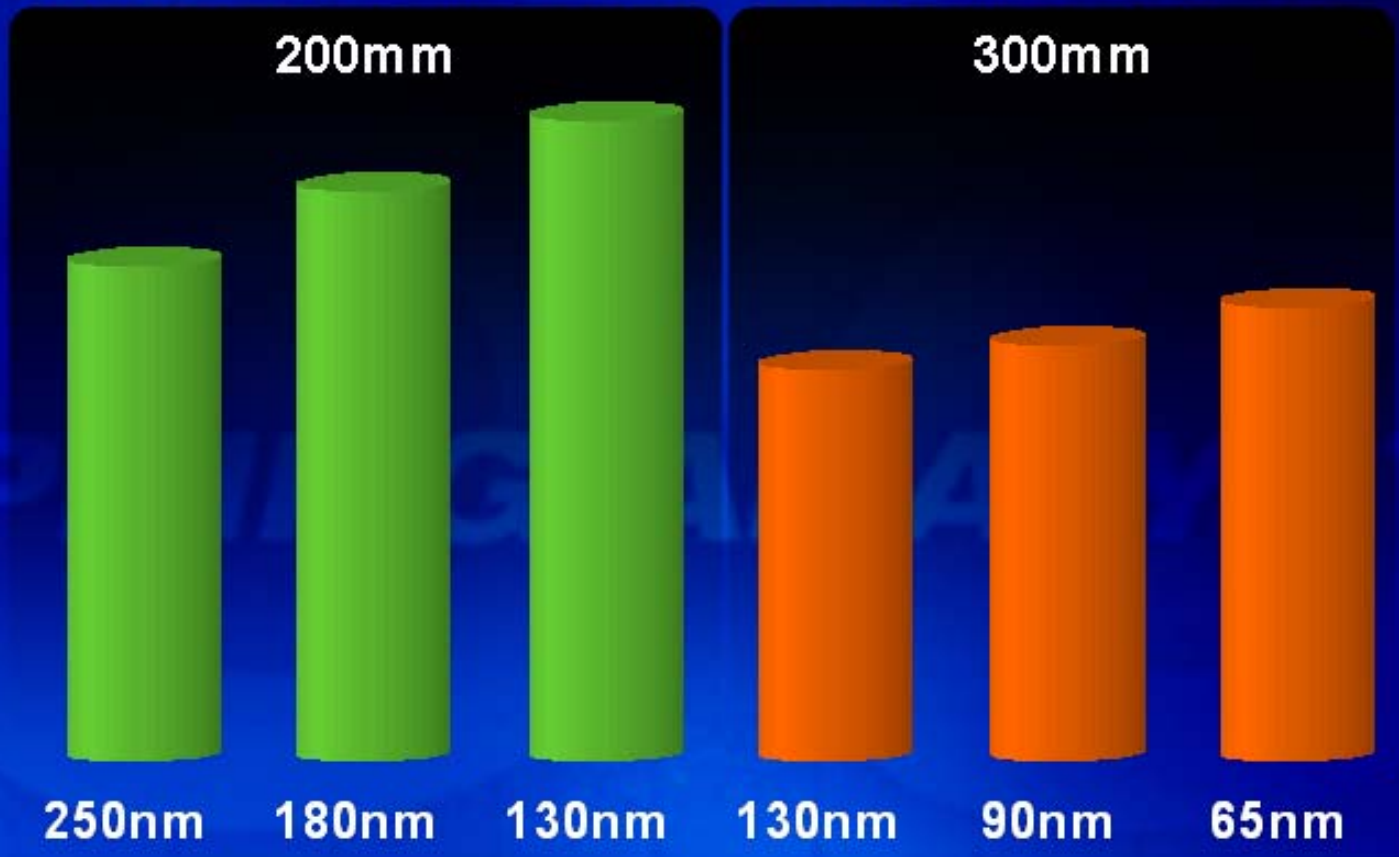


Converting to 65nm → ~$2B Net Savings

Source: Intel

300mm Rolls Back Costs

Capital Cost per Square Inch of Wafer Area* ($) (Projected)



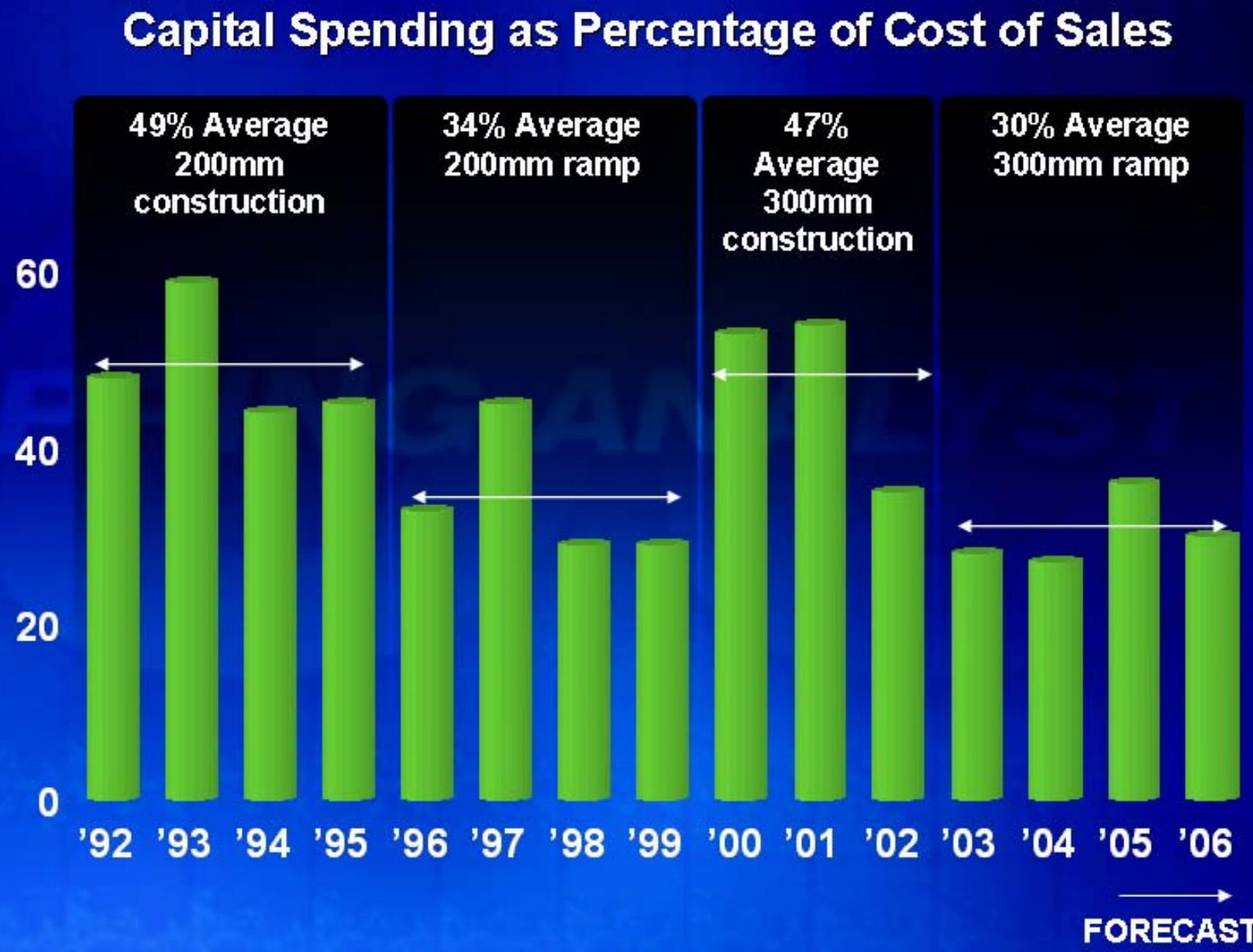
The number of transistors per sq. inch today (65nm) is 100-fold higher than 10 years ago (250nm)

intel

*Total CPU projected shipments

Source: Intel

Capital Intensity as 300mm Ramps



Source: Intel

300mm Economies of Scale Achieved Only at High Volumes

FAB	$3B
PILOT LINE	$1-2B
R&D PROCESS TEAM	$0.5-1B

$5B investment requires high volume to achieve reasonable unit cost

intel

Source: Intel

Wafer Capacity Investment Strategy



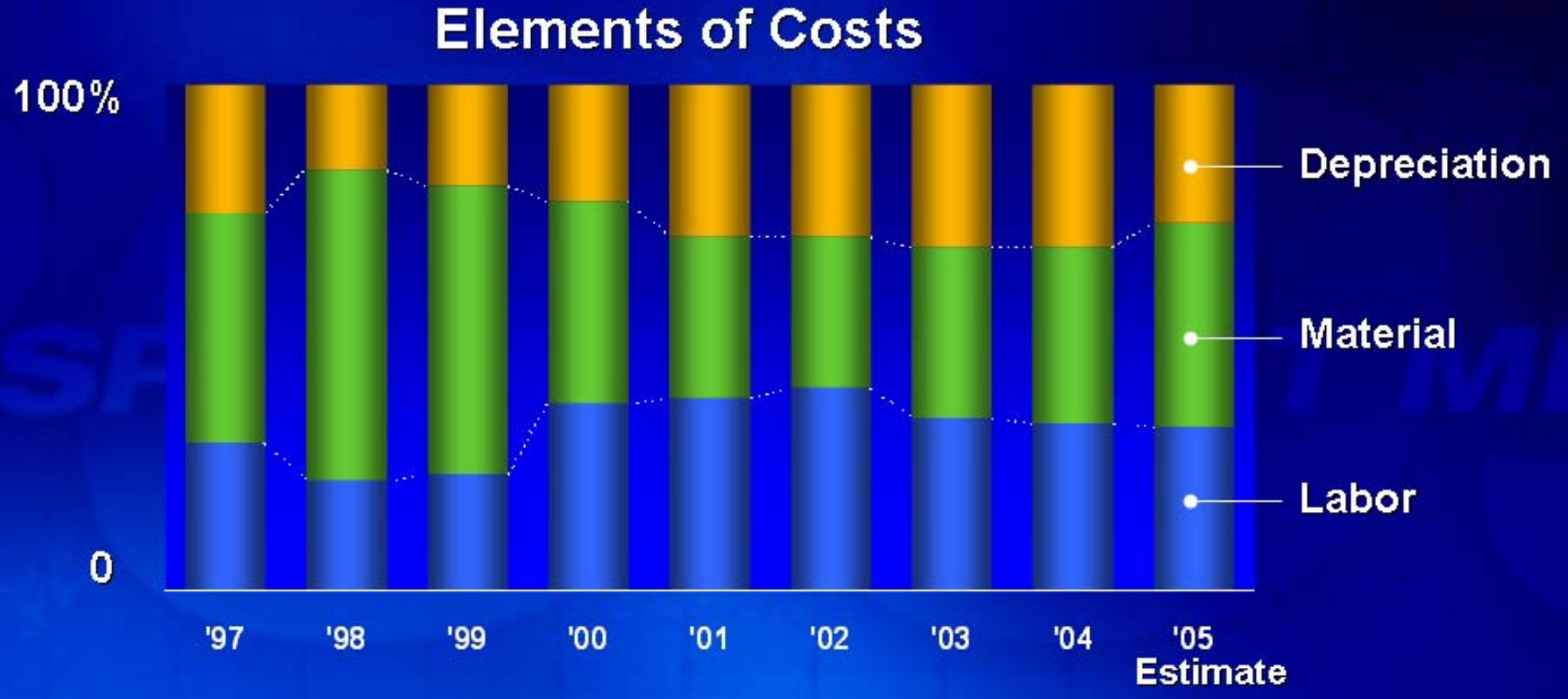
"Capacity is strategy."
–Henry Ford

"Strategy is destiny."
–Dr. Robert Burgelman

intel

Source: Intel

Elements of Microprocessor Unit Costs



300mm → Depreciation down

intel

Source: Intel

Microprocessor Unit Costs Trend Down

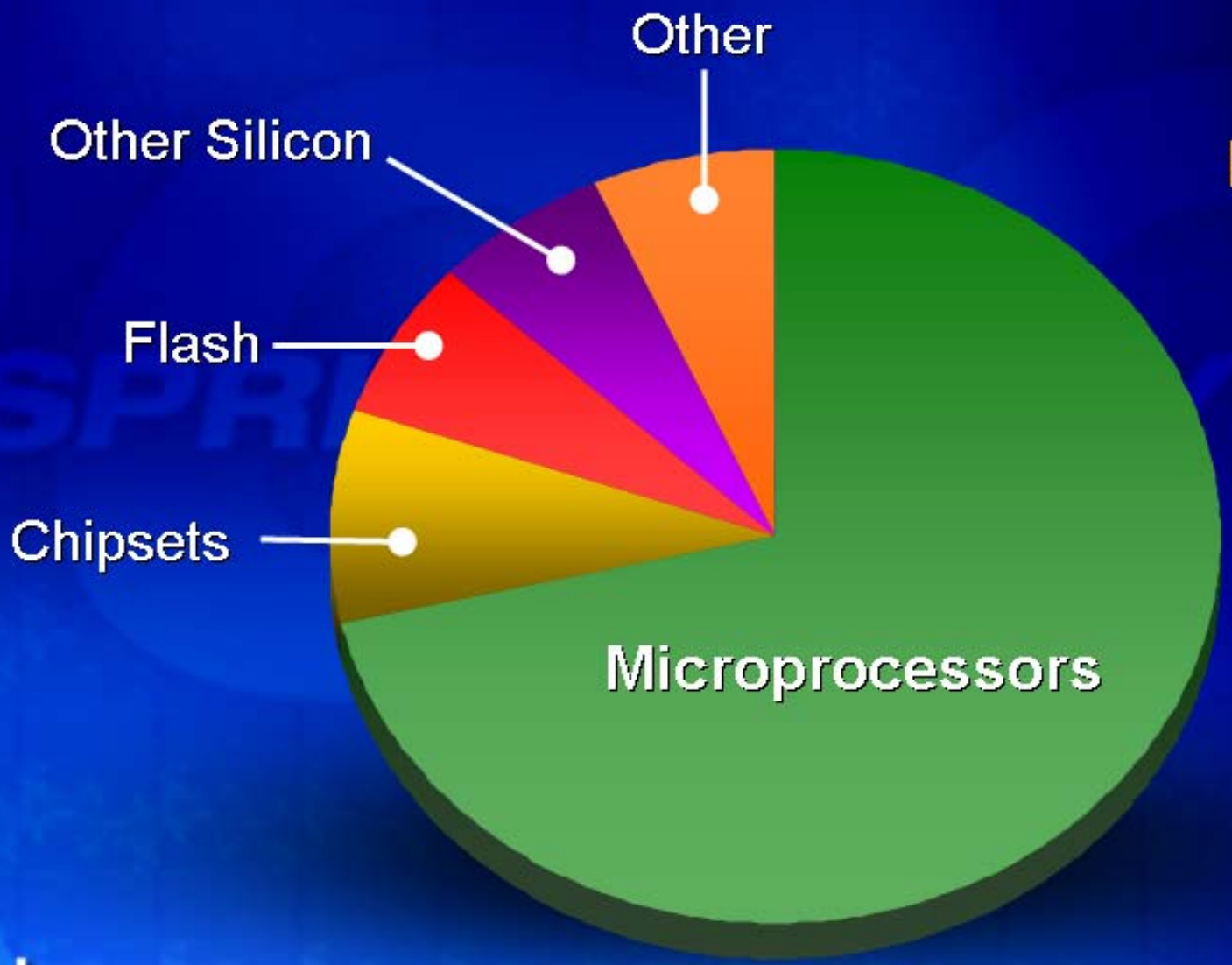


Plan to achieve ~25% reduction 2004 – 2006

intel

Source: Intel

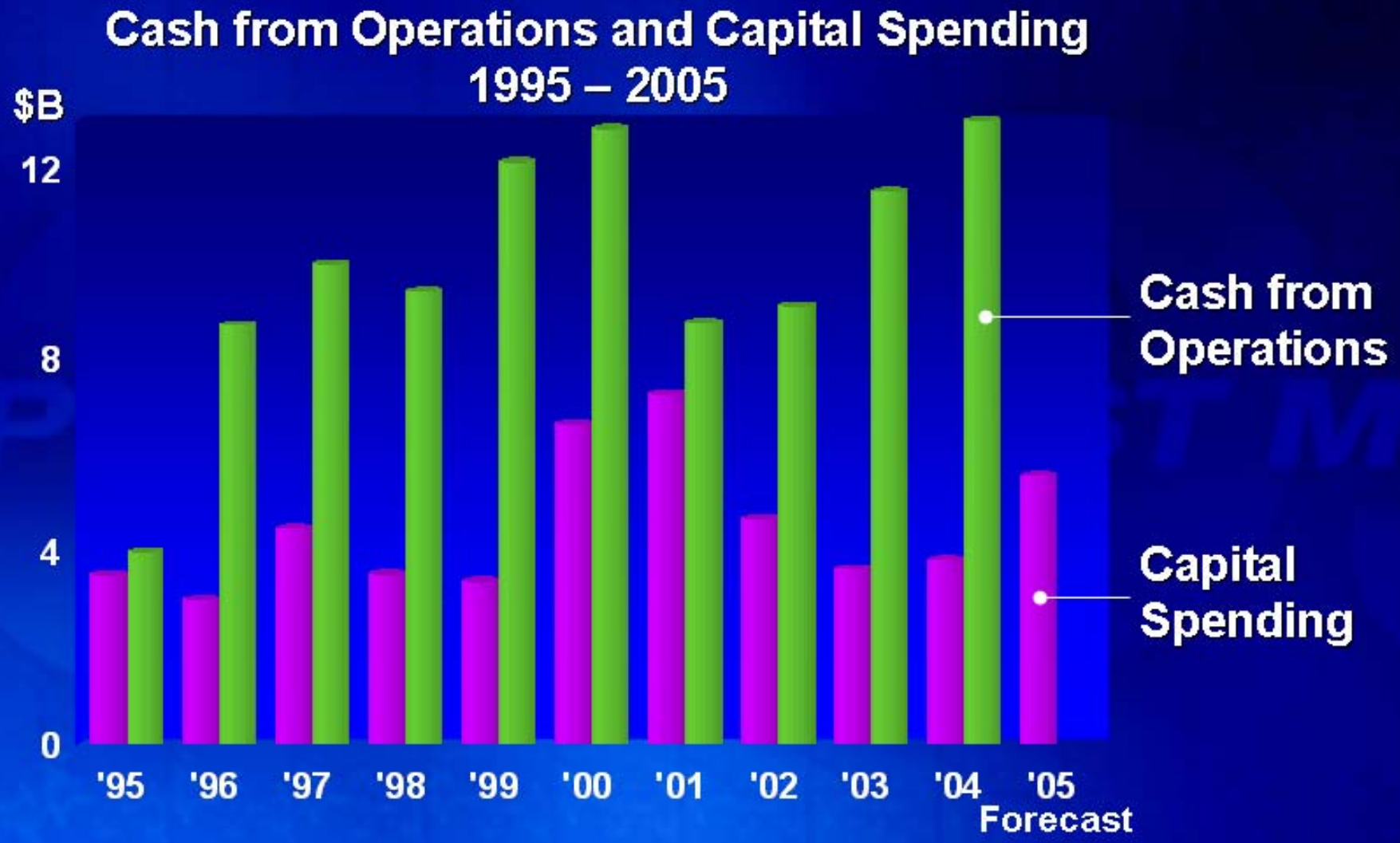
Platform Ingredients



Revenue by Product
2004

Source: Intel

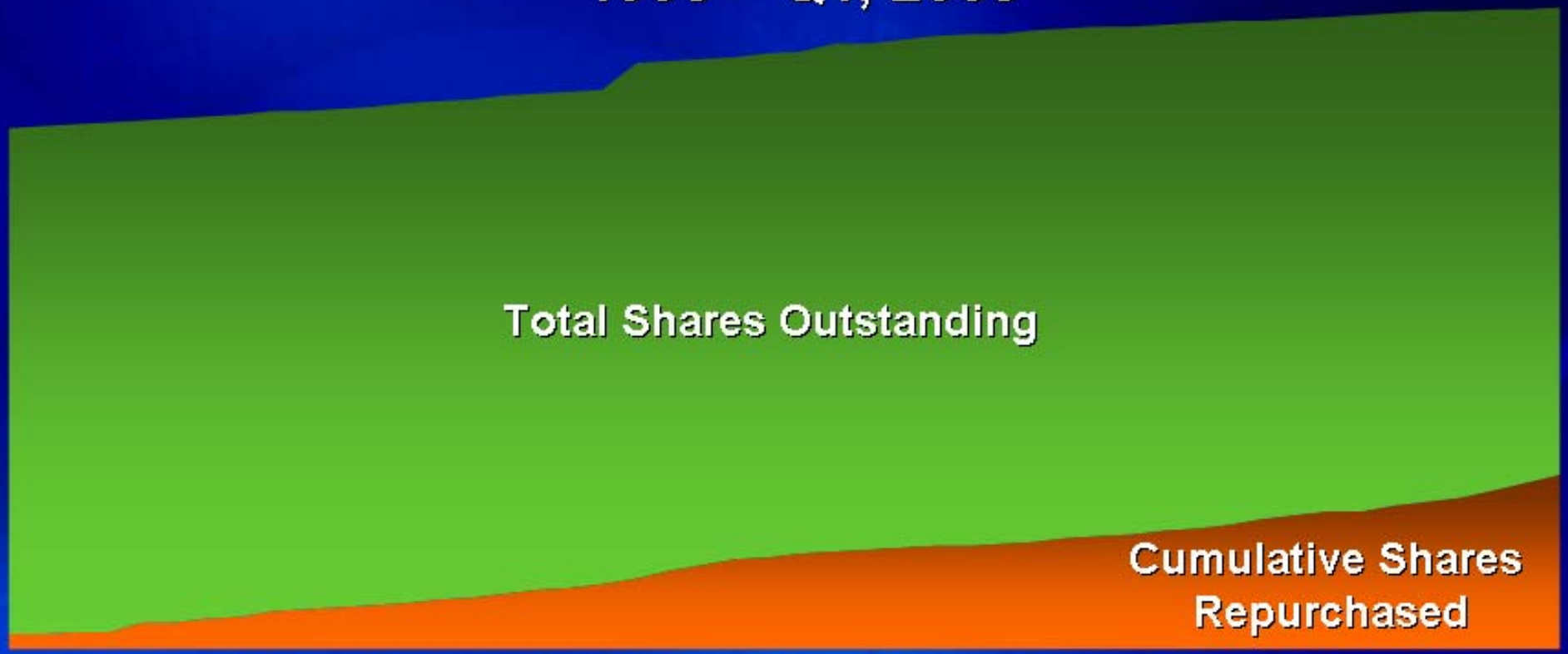
Generating Cash



Source: Intel

Returning Cash to Stockholders:
Stock Repurchase

1993 – Q1, 2005



Cumulative 2.3B shares repurchased = 27% of total
Share count down 9% from peak

intel

Source: Intel

Returning Cash to Stockholders:
Cash Dividends

1992 – Q1, 2005

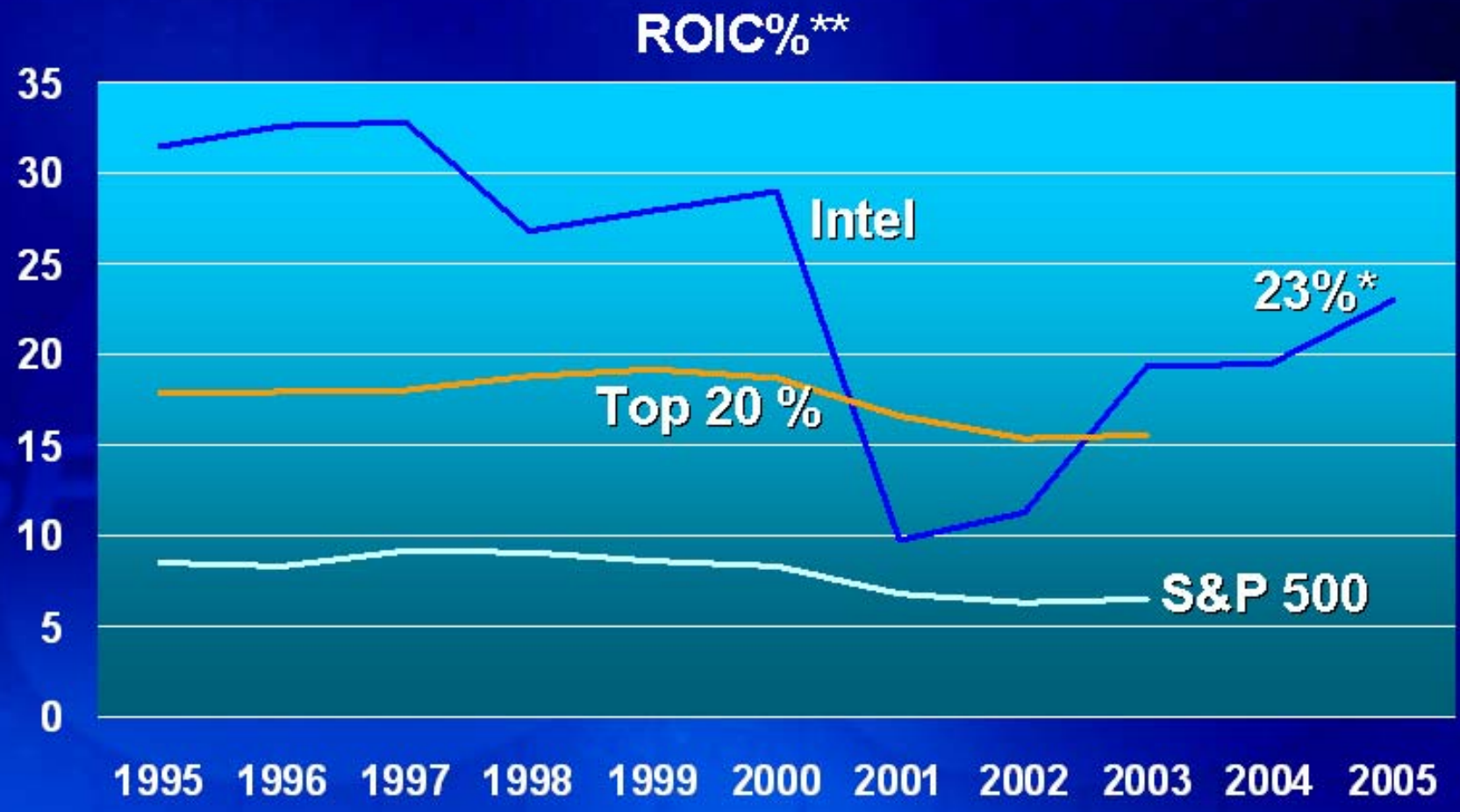


$4.8B in Cumulative Payments

intel

Source: Intel

ROIC Progress Report



Long term goal to rank among top ROIC performers
10 years ~24% 2001 & 2002 ~10-11% 2003 & 2004 ~19%

intel

*2005 figure for return on invested capital is not an Intel forecast but represents the Q1 2005 figures multiplied by four.
**ROIC includes cash and goodwill; from 1993 to 1996, ROIC includes marketable equity securities.
Source: Intel